Dual Very Low Noise Precision Operational Amplifier

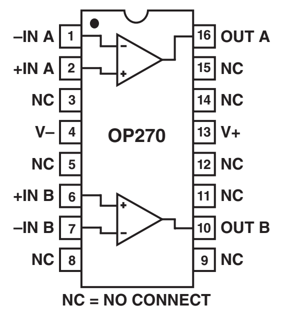
OP270

FEATURES

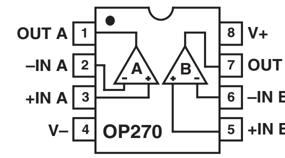
- Very Low Noise 5 nV/√Hz @ 1 kHz Max
- Excellent Input Offset Voltage 75 μV Max
- Low Offset Voltage Drift 1 μV/°C Max
- Very High Gain 1500 V/mV Min
- Outstanding CMR 106 dB Min
- Slew Rate 2.4 V/μs Typ
- Gain Bandwidth Product 5 MHz Typ
- Industry-Standard 8-Lead Dual Pinout

CONNECTION DIAGRAMS

16-Lead SOIC (S-Suffix)



8-Lead PDIP (P-Suffix)
8-Lead CERDIP (Z-Suffix)



GENERAL DESCRIPTION

The OP270 is a high performance, monolithic, dual operational amplifier with exceptionally low voltage noise, 5 nV/√Hz max at 1 kHz. It offers comparable performance to ADI's industry standard OP27.

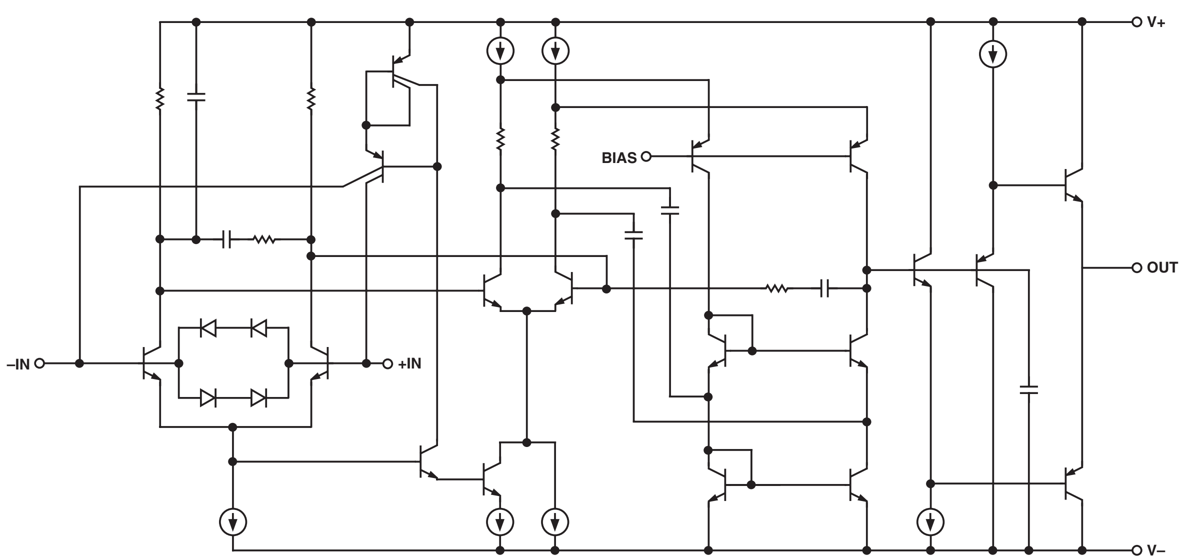
The OP270 features an input offset voltage below 75 μV and an offset drift under 1 μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP270 is over 1,500,000 into a 10 kΩ load, ensuring excellent gain accuracy and linearity, even in high gain applications. Input bias current is under 20 nA, which reduces errors due to signal source resistance. The OP270's CMR of over 106 dB and PSRR of less than 3.2 μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the dual OP270 is one-third less than two OP27s, a significant advantage for power conscious applications. The OP270 is unity-gain stable with a gain bandwidth product of 5 MHz and a slew rate of 2.4 V/μs.

The OP270 offers excellent amplifier matching, which is important for applications such as multiple gain blocks, low noise instrumentation amplifiers, dual buffers, and low noise active filters.

The OP270 conforms to the industry-standard 8-lead DIP pinout. It is pin compatible with the MC1458, SE5532/A, RM4558, and HA5102 dual op amps, and can be used to upgrade systems using those devices.

For higher speed applications, the OP271, with a slew rate of 8 V/μs, is recommended. For a quad op amp, see the OP470.

SIMPLIFIED SCHEMATIC
(One of Two Amplifiers Is Shown)



REV. C

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OP270–SPECIFICATIONS (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP270E MIN	OP270E TYP	OP270E MAX	OP270F MIN	OP270F TYP	OP270F MAX	OP270G MIN	OP270G TYP	OP270G MAX	UNIT
Input Offset Voltage	V_{OS}			10	75		20	150		50	250	µV
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	10		3	15		5	20	nA
Input Bias Current	I_B	V_{CM} = 0 V		5	20		10	40		15	60	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz (Note 1)		80	200		80	200		80		nV p-p
Input Noise Voltage Density		f_O = 10 Hz		3.6	6.5		3.6	6.5		3.6		nV/√Hz
		f_O = 100 Hz		3.2	5.5		3.2	5.5		3.2		nV/√Hz
	e_n	f_O = 1 kHz (Note 2)		3.2	5.0		3.2	5.0		3.2		nV/√Hz
Input Noise Current Density		f_O = 10 Hz		1.1			1.1			1.1		pA/√Hz
	i_n	f_O = 100 Hz		0.7			0.7			0.7		pA/√Hz
		f_O = 1 kHz		0.6			0.6			0.6		pA/√Hz
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 10 kΩ	1500	2300		1000	1700		750	1500		V/mV
		R_L = 2 kΩ	750	1200		500	900		350	700		V/mV
Input Voltage Range	IVR	(Note3)	±12	±12.5		±12	±12.5		±12	±12.5		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	106	125		100	120		90	110		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.56	3.2		1.0	5.6		1.5	6	µV/V
Slew Rate	SR		1.7	2.4		1.7	2.4		1.7	2.4		V/µs
Supply Current (All Amplifiers)	I_{SY}	No Load		4	6.5		4	6.5		4	6.5	mA
Gain Bandwidth Product	GBP			5			5			5		MHz
Channel Separation	CS	V_O = ±20 V p-p, f_O = 10 Hz (Note 1)	125	175		125	175			175		dB
Input Capacitance	C_{IN}			3			3			3		pF
Input Resistance Differential-Mode	R_{IN}			0.4			0.4			0.4		MΩ
Input Resistance Common-Mode	R_{INCM}			20			20			20		GΩ
Settling Time	t_S	A_V = +1, 10 V Step to 0.01%		5			5			5		µs

NOTES
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

Specifications subject to change without notice.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (Vs = ±15 V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP270E MIN	OP270E TYP	OP270E MAX	OP270F MIN	OP270F TYP	OP270F MAX	OP270G MIN	OP270G TYP	OP270G MAX	UNIT
Input Offset Voltage	V_{OS}			25	150		45	275		100	400	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.2	1		0.4	2		0.7	3	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		1.5	30		5	40		15	50	nA
Input Bias Voltage	I_B	V_{CM} = 0 V		6	60		15	70		19	80	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 10 kΩ	1000	1800		600	1400		400	1250		V/mV
		R_L = 2 kΩ	500	900		300	700		225	670		V/mV
Input Voltage Range*	IVR		±12	±12.5		±12	±12.5		±12	±12.5		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	100	120		94	115		90	100		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.7	5.6		1.8	10		2.0	1.5	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load		4.4	7.2		4.4	7.2		4.4	7.2	mA

* Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Differential Input Voltage[2] . . . . ±1.0 V
Differential Input Current[2] . . . . ±25 mA
Input Voltage . . . . Supply Voltage
Output Short-Circuit Duration . . . . Continuous
Storage Temperature Range
  P, S, Z Package . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . 300°C
Junction Temperature (T_J) . . . . –65°C to +150°C
Operating Temperature Range
  OP270E, OP270F, OP270G . . . . –40°C to +85°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] The OP270's inputs are protected by back-to-back diodes. Current limiting resistors are not used, in order to achieve low noise performance. If differential voltage exceeds +10 V, the input current should be limited to ±25 mA.

ORDERING GUIDE

Model	T_A = +25°C V_{OS} Max (µV)	θ_{JC} (°C/W)	θ_{JA}* (°C/W)	Temperature Range	Package Description	Package Option
OP270EZ	75	12	134	XIND	8-Lead CERDIP	Q-8 (Z-Suffix)
OP270FZ	150	12	134	XIND	8-Lead CERDIP	Q-8 (Z-Suffix)
OP270GP	250	37	96	XIND	8-Lead PDIP	N-8 (P-Suffix)
OP270GS	250	27	92	XIND	16-Lead SOIC	RW-16 (S-Suffix)

*θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

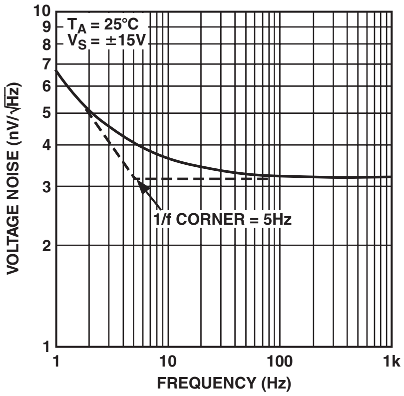
For military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp.

SMD Part Number	ADI Equivalent
5962-8872101PA	OP270AZMDA

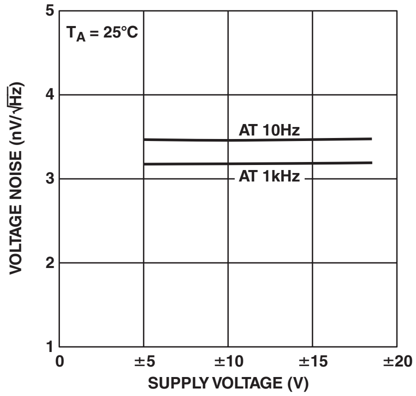
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP270 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

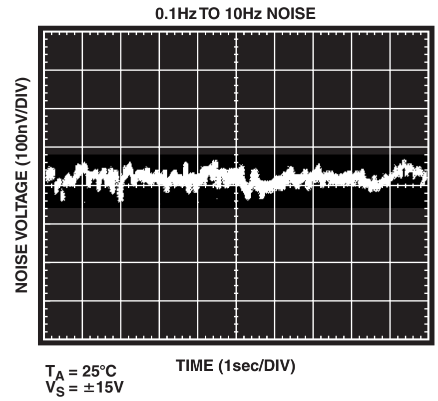




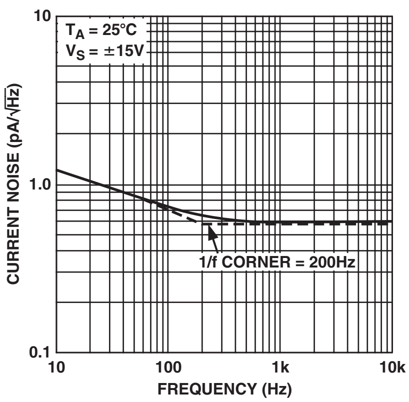
TPC 1. Voltage Noise Density vs. Frequency



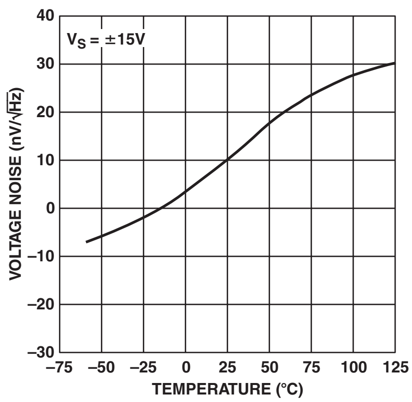
TPC 2. Voltage Noise Density vs. Supply Voltage



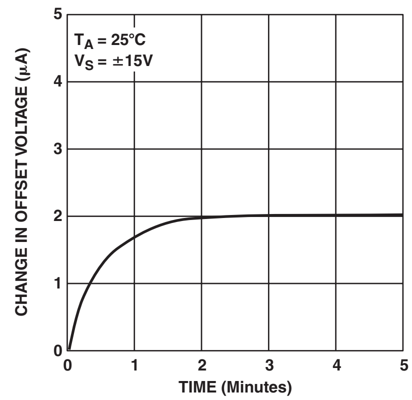
TPC 3. 0.1 Hz to 10 Hz Input Voltage Noise



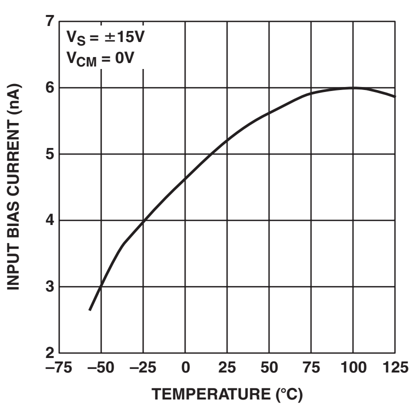
TPC 4. Current Noise Density vs. Frequency



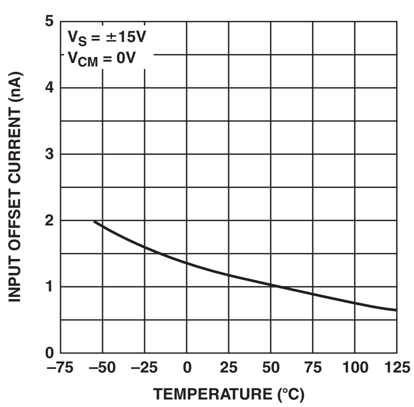
TPC 5. Input Offset Voltage vs. Temperature



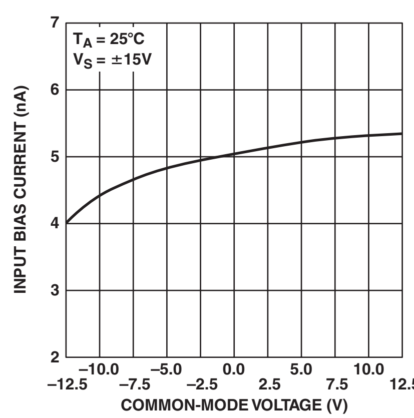
TPC 6. Warm-Up Offset Voltage Drift



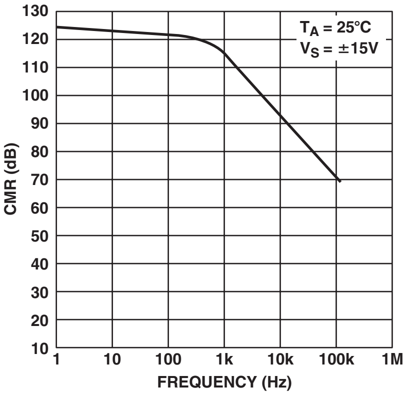
TPC 7. Input Bias Current vs. Temperature



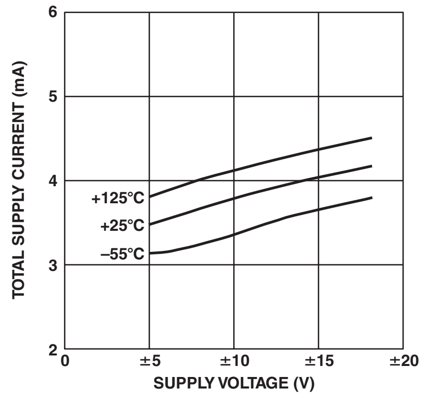
TPC 8. Input Offset Current vs. Temperature



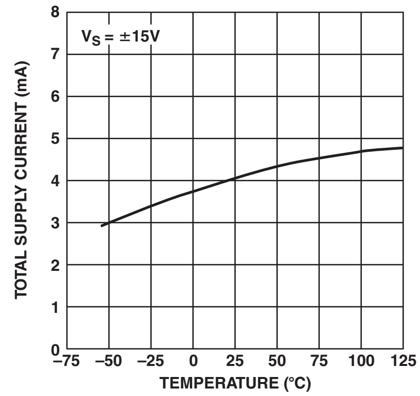
TPC 9. Input Bias Current vs. Common-Mode Voltage



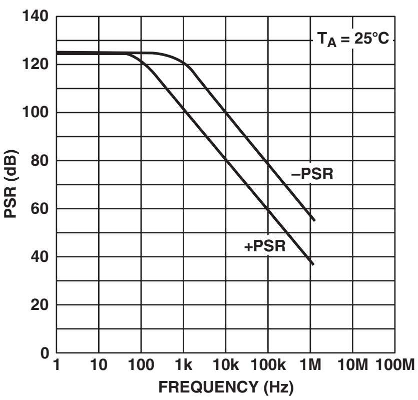
TPC 10. CMR vs. Frequency



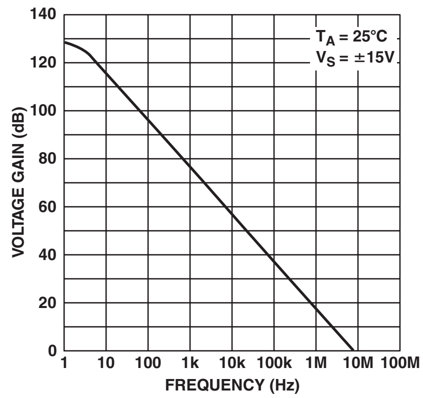
TPC 11. Total Supply Current vs. Supply Voltage



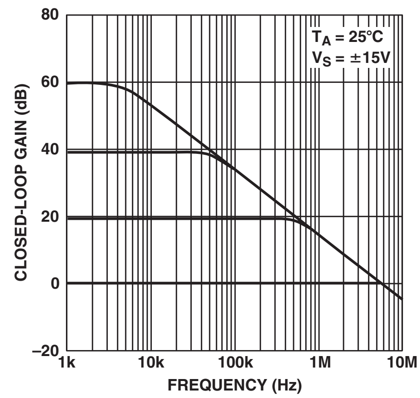
TPC 12. Total Supply Current vs. Temperature



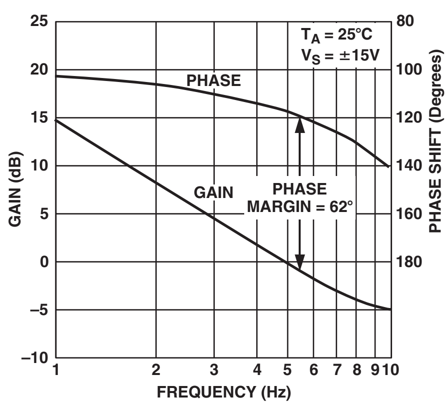
TPC 13. PSR vs. Frequency



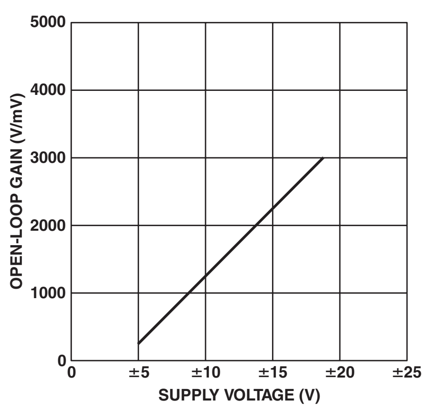
TPC 14. Open-Loop Gain vs. Frequency



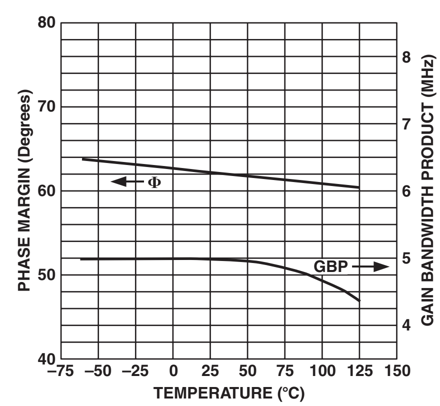
TPC 15. Closed-Loop Gain vs. Frequency



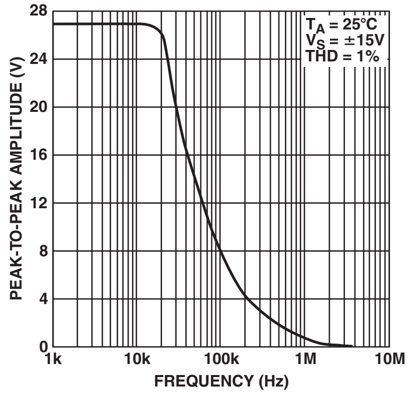
TPC 16. Open-Loop Gain Phase Shift vs. Frequency



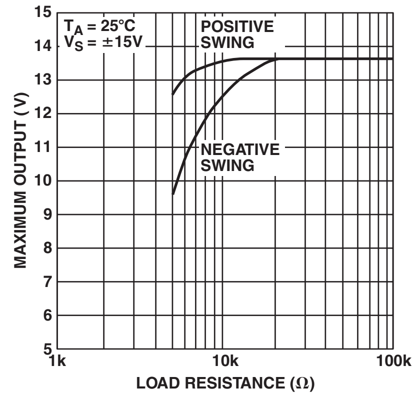
TPC 17. Open-Loop Gain vs. Supply Voltage



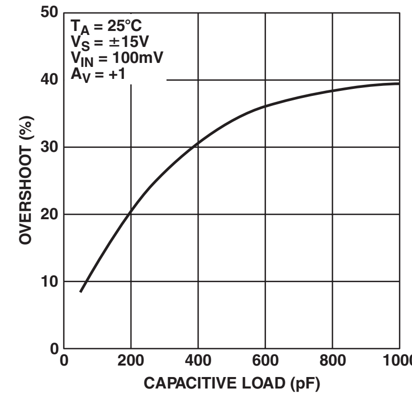
TPC 18. Gain-Bandwidth Phase Margin vs. Temperature



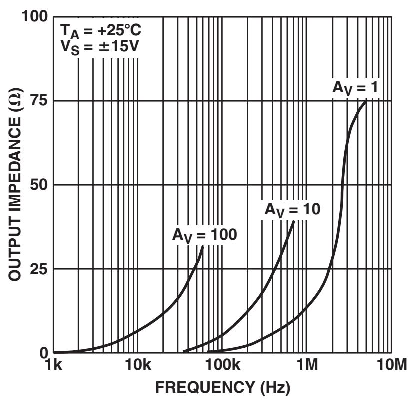
TPC 19. Maximum Output Swing vs. Frequency



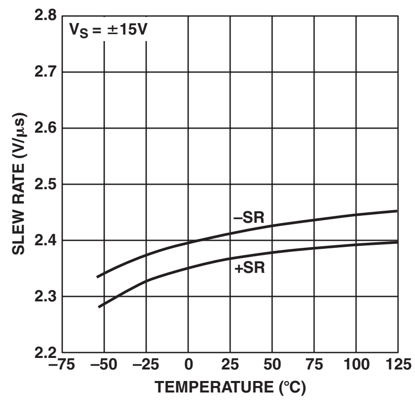
TPC 20. Maximum Output Voltage vs. Load Resistance



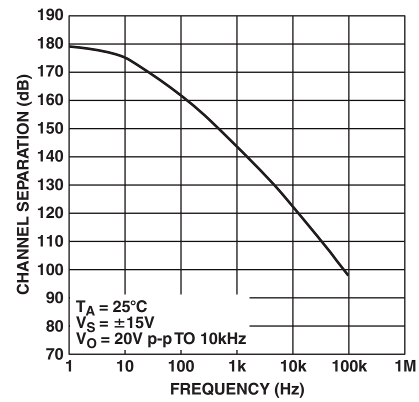
TPC 21. Small-Signal Overshoot vs. Capacitive Load



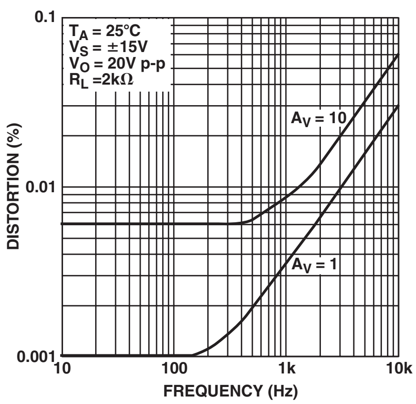
TPC 22. Output Impedance vs. Frequency



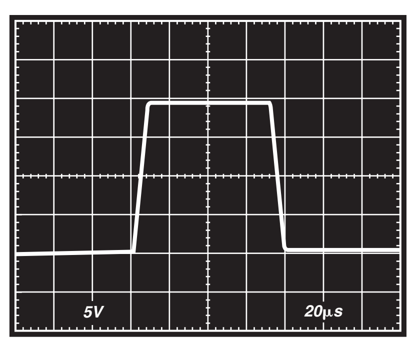
TPC 23. Slew Rate vs. Temperature



TPC 24. Channel Separation vs. Frequency

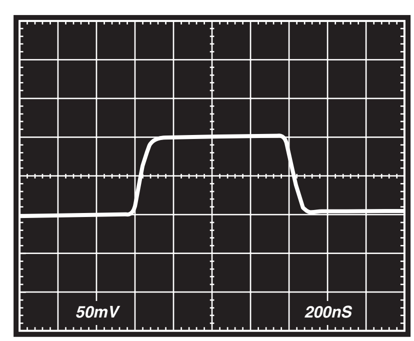


TPC 25. Total Harmonic Distortion vs. Frequency



T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 2kΩ

TPC 26. Large Signal Transcient Response



T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 2kΩ

TPC 27. Small-Signal Transient Response

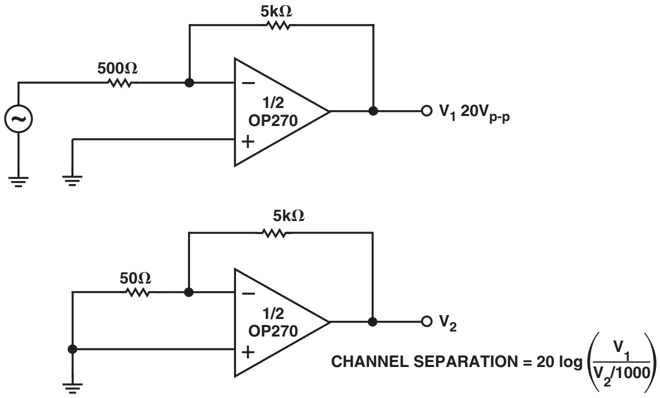


Figure 1. Channel Separation Test Circuit

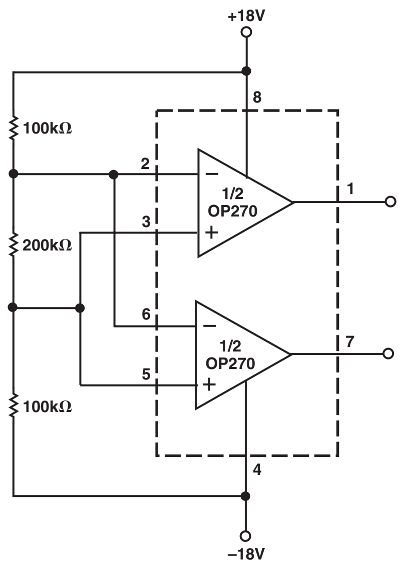


Figure 2. Burn-In Circuit

APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP270 is a very low noise dual op amp, exhibiting atypical voltage noise of only 3.2 nV/$\sqrt{\text{Hz}}$ @ 1 kHz. The exceptionally low noise characteristic of the OP270 is achieved in part by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP270 is gained at the expense of current noise performance, which is normal for low noise amplifiers.

To obtain the best noise performance in a circuit, it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 3 shows the relationship between total noise at 1 kHz and source resistance. For R_S < 1 kΩ the total noise is dominated by the voltage noise of the OP270. As R_S rises above 1 kΩ, total noise increases and is dominated by resistor noise rather than by the voltage or current noise of the OP270. When R_S exceeds 20 kΩ, current noise of the OP270 becomes the major contributor to total noise.

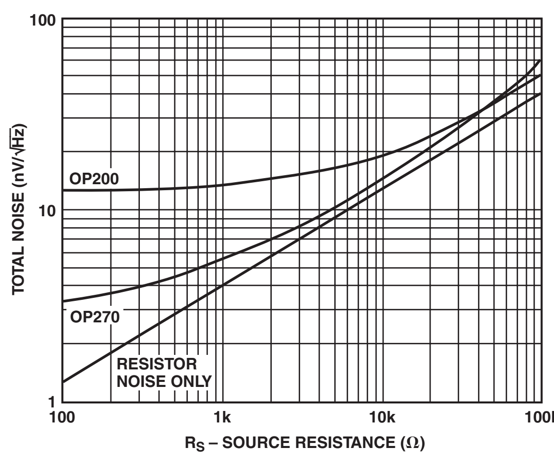


Figure 3. Total Noise vs. Source Resistance (Including Resistor Noise) at 1 kHz

Figure 4 also shows the relationship between total noise and source resistance, but at 10 Hz. Total noise increases more quickly than shown in Figure 3 because current noise is inversely proportional to the square root of frequency. In Figure 4, current noise of the OP270 dominates the total noise when R_S > 5 kΩ.

Figures 3 and 4 show that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP200, with lower current noise than the OP270, will provide lower total noise.

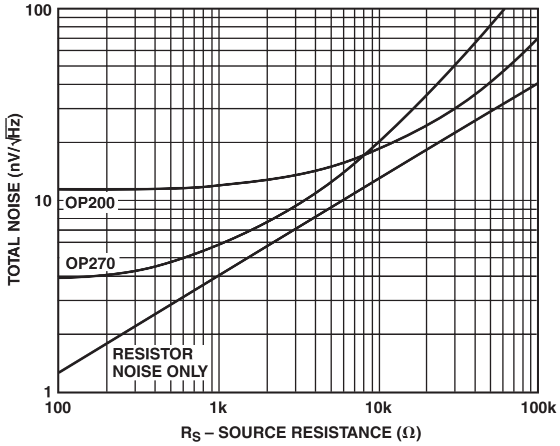


Figure 4. Total Noise vs. Source Resistance (Including Resistor Noise) at 10 Hz

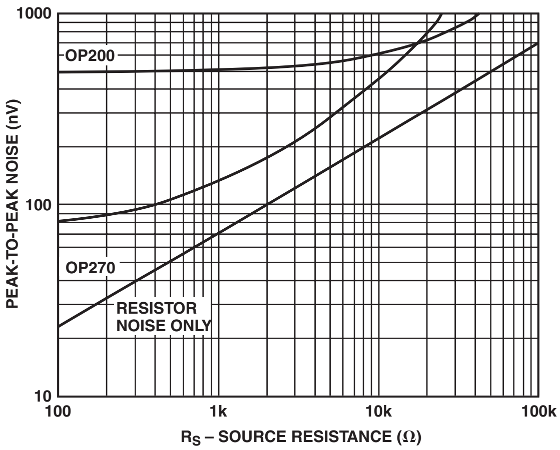


Figure 5. Peak-to-Peak Noise (0.1 Hz to 10 Hz) vs. Source Resistance (Includes Resistor Noise)

Figure 5 shows peak-to-peak noise versus source resistance over the 0.1 Hz to 10 Hz range. Once again, at low values of R_S, the voltage noise of the OP270 is the major contributor to peak-to-peak noise, with current noise the major contributor as R_S increases. The crossover point between the OP270 and the OP200 for peak-to-peak noise is at R_S = 17 kΩ.

The OP271 is a higher speed version of the OP270, with a slew rate of 8 V/μs. Noise of the OP271 is slightly higher than that of the OP270. Like the OP270, the OP271 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table I.

Table I.

Device	Source Impedance	Comments
Strain gage	<500 Ω	Typically used in low frequency applications.
Magnetic tapehead, microphone	<1500 Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP270 I_B can be neglected.
Magnetic phonograph cartridge	<1500 Ω	Similar need for low I_B in direct coupled applications. OP270 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500 Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400 Hz to 5 kHz.

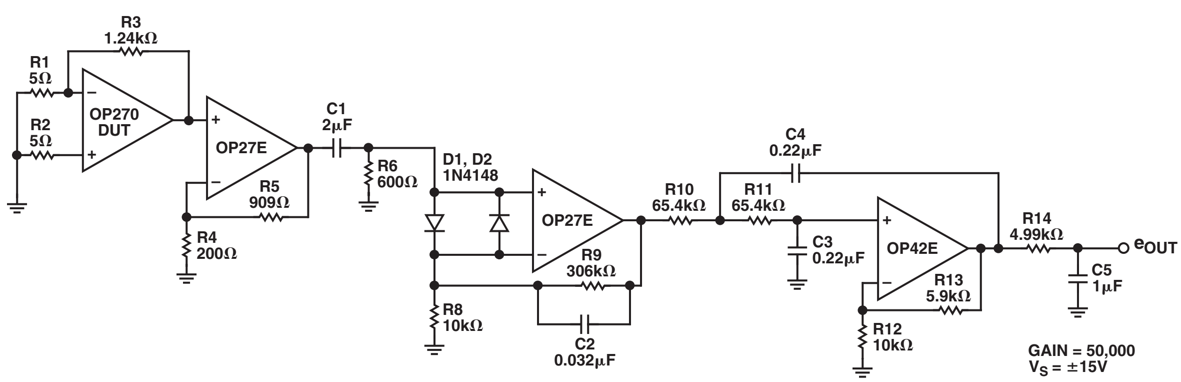


Figure 6. Peak-to-Peak Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

NOISE MEASUREMENTS

Peak-to-Peak Voltage Noise

The circuit of Figure 6 is a test setup for measuring peak-to-peak voltage noise. To measure the 200 nV peak-to-peak noise specification of the OP270 in the 0.1 Hz to 10 Hz range, the following precautions must be observed:

1. The device has to be warmed up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 2 µV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature induced effects can exceed tens of nanovolts.
2. For similar reasons, the device has to be well shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed through" to increase the observed noise.
4. The test time to measure noise of 0.1 Hz to 10 Hz should not exceed 10 seconds. As shown in the noise-tester frequency response curve of Figure 7, the 0.1 Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1 Hz.

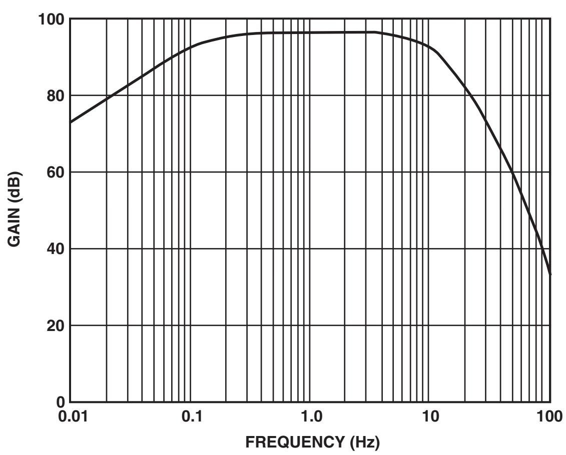


Figure 7. 0.1 Hz to 10 Hz Peak-to-Peak Voltage Noise Test Circuit Frequency Response

5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage-density measurement will correlate well with a 0.1 Hz to 10 Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low noise supplies, e.g., batteries. They will minimize output noise introduced via the amplifier supply pins.

Noise Measurement — Noise Voltage Density

The circuit of Figure 8 shows a quick and reliable method of measuring the noise voltage density of dual op amps. The first amplifier is in unity-gain, with the final amplifier in a noninverting gain of 101. As noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\left(\sqrt{\left(e_{nA}\right)^2 + \left(e_{nB}\right)^2}\right)$$

The OP270 is a monolithic device with two identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\left(\sqrt{2e_n^{\,2}}\right) = 101\left(\sqrt{2}e_n\right)$$

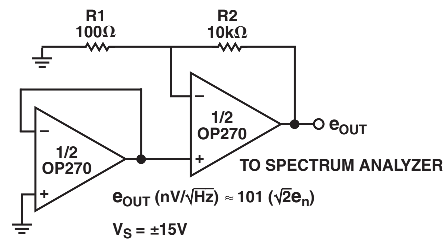


Figure 8. Noise Voltage Density Test Circuit

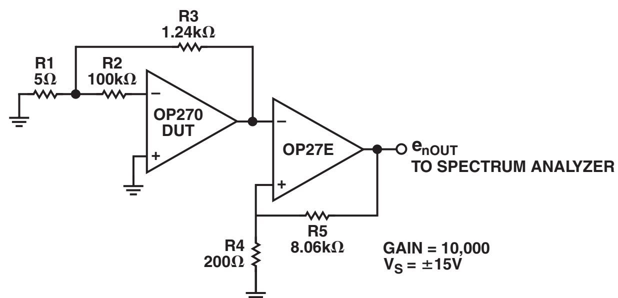


Figure 9. Current Noise Density Test Circuit

Noise Measurement — Current Noise Density

The test circuit shown in Figure 9 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40\ nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10,000
R_S = 100 kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP270 is unity-gain stable and capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP270.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 10. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 10 are for a load capacitance of up to 1,000 pF when used with the OP270.

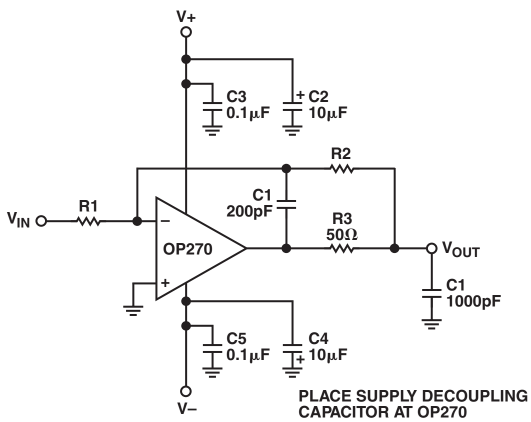


Figure 10. Driving Large Capacitive Loads

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\ \Omega$ and the input is driven with a fast, large signal pulse (>1 V), the output waveform will look like the one in Figure 11.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3\ k\Omega$, a pole created by R_f and the amplifier's input capacitance (3 pF) creates additional phase shift and reduces phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_f helps eliminate this problem.

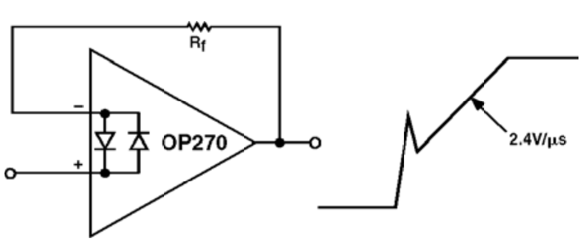


Figure 11. Pulsed Operation

APPLICATIONS

Low Phase Error Amplifier

The simple amplifier depicted in Figure 12 utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $Vo/(K1 + 1) = V_2/(K1 + 1)$, yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The dc gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note that like a conventional single op amp amplifier, the dc gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

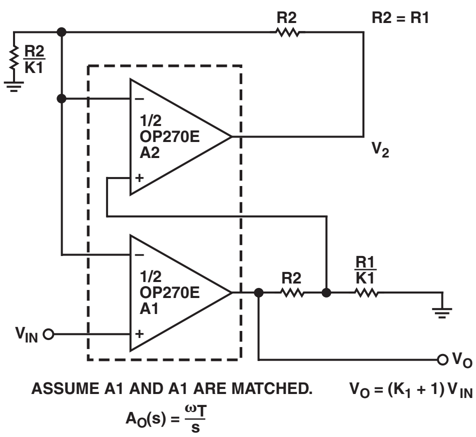


Figure 12. Low Phase Error Amplifier

Figure 13 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of –0.1° occurs at 0.002 $\omega/\beta\omega_T$ for the single op amp amplifier, but at 0.11 $\omega/\beta\omega_T$ for the low phase error amplifier.

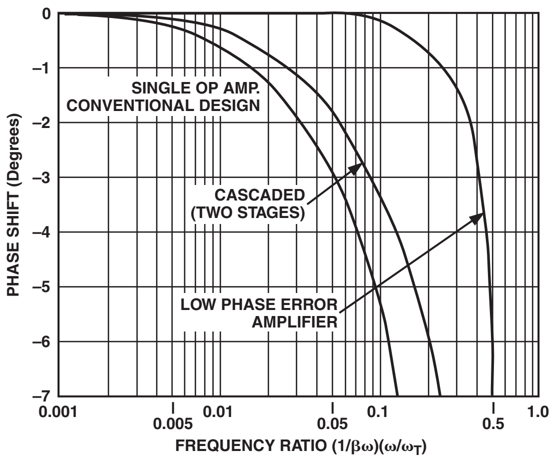


Figure 13. Phase Error Comparison

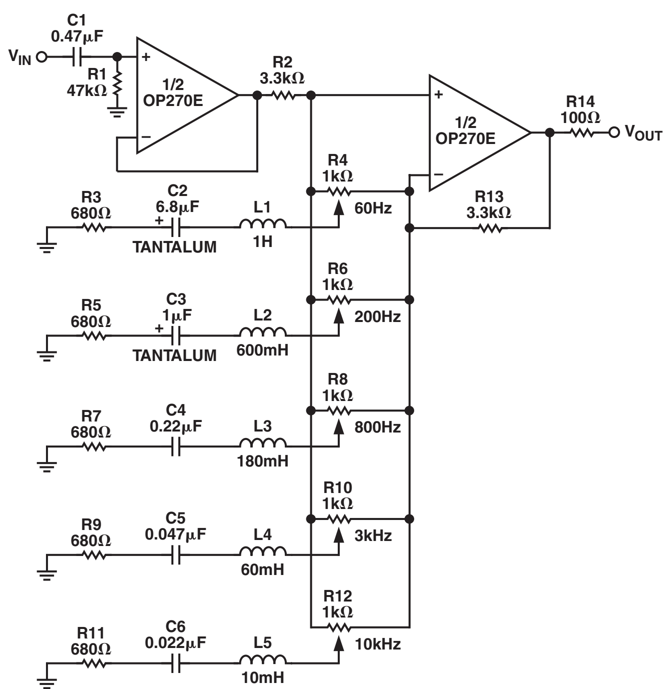


Figure 14. 5-Band Low Noise Graphic Equalizer

FIVE-BAND LOW NOISE STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 14 provides 15 dB of boost or cut over a 5-band range. Signal-to-noise ratio over a 20 kHz bandwidth is better than 100 dB and referred to a 3 V rms input. Larger inductors can be replaced by active inductors, but this reduces the signal-to-noise ratio.

DIGITAL PANNING CONTROL

Figure 15 uses a DAC8221, a dual 12-bit CMOS DAC, to pan a signal between two channels. One channel is formed by the current output of DAC A driving one-half of an OP270 in a current-to-voltage converter configuration. The other channel is formed by the complementary output current of DAC A, which normally flows to ground through the AGND pin. This complementary current is converted to a voltage by the other half of the OP-270, which also holds AGND at virtual ground.

Gain error due to mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC8221. Only DAC A passes a signal; DAC B provides the second feedback resistor. With $V_{REF}B$ unconnected, the current-to-voltage converter, using $R_{FB}B$, is accurate and not influenced by digital data reaching DAC B. Distortion of the digital panning control is less than 0.002% over the 20 Hz to 20 kHz audio range. Figure 16 shows the complementary outputs for a 1 kHz input signal and a digital ramp applied to the DAC data input.

DUAL PROGRAMMABLE GAIN AMPLIFIER

The dual OP270 and the DAC8221, a dual 12-bit CMOS DAC, can be combined to form a space-saving dual programmable amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the internal feedback resistor and the resistance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is

$$\frac{V_{OUT}}{V_{IN}} = -\frac{4096}{n}$$

where n equals the decimal equivalent of the 12-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will open, causing the op amp output to saturate. A 20 MΩ resistor placed in parallel with the DAC feedback loop eliminates this problem with only a very small reduction in gain accuracy.

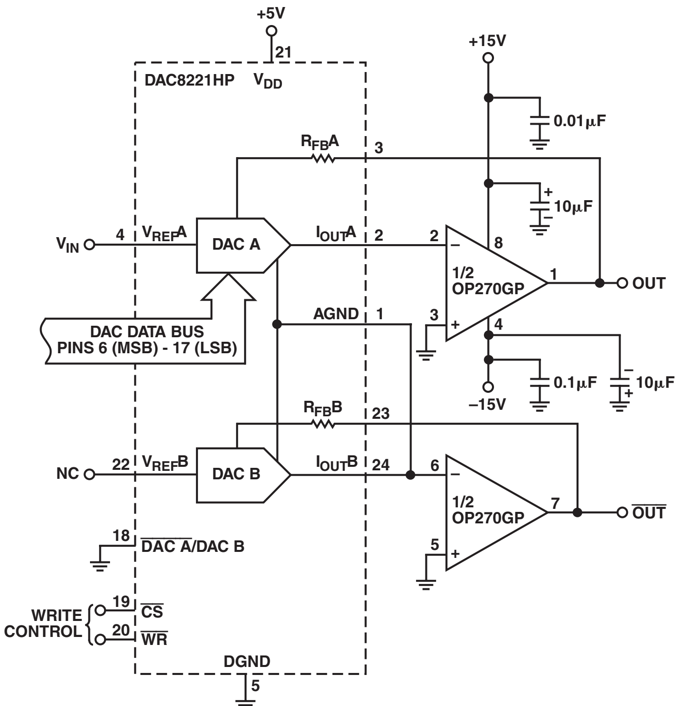


Figure 15. Digital Panning Control

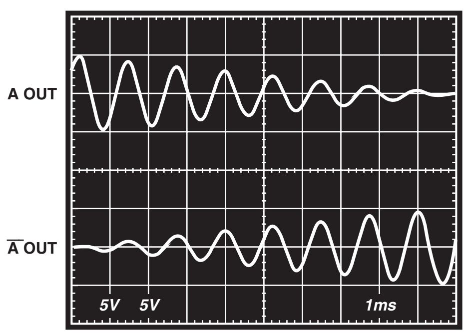


Figure 16. Digital Panning Control Output

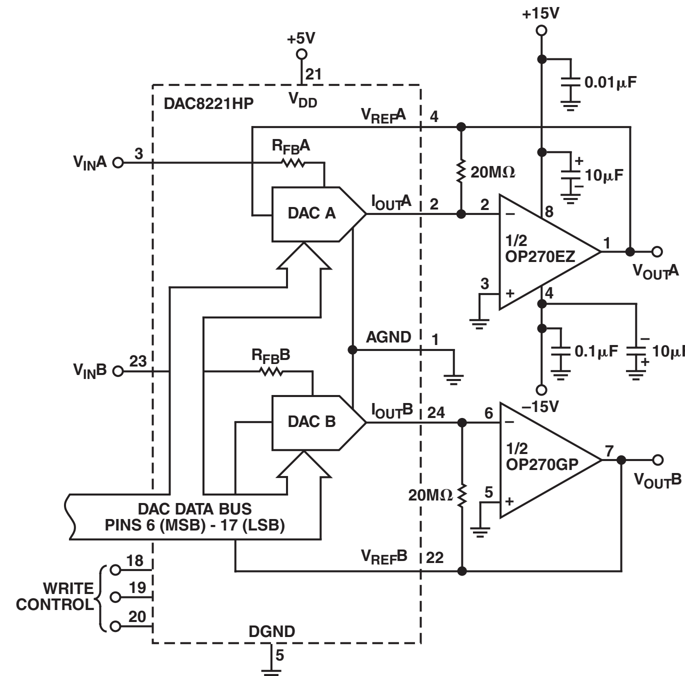
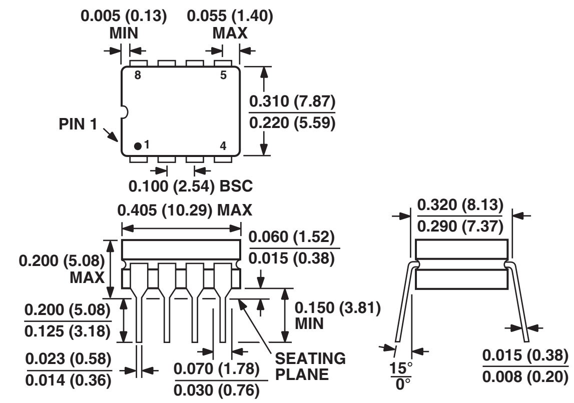


Figure 17. Dual Programmable Gain Amplifier

OUTLINE DIMENSIONS

8-Lead Ceramic Dual In-Line Package [CERDIP] Z-Suffix (Q-8)

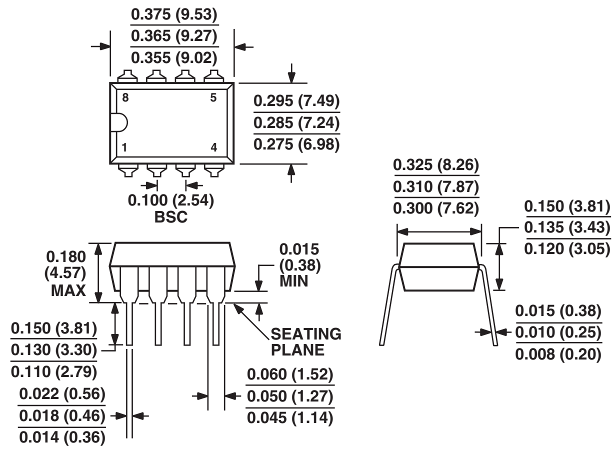
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual In-Line Package [PDIP] P-Suffix (N-8)

Dimensions shown in inches and (millimeters)

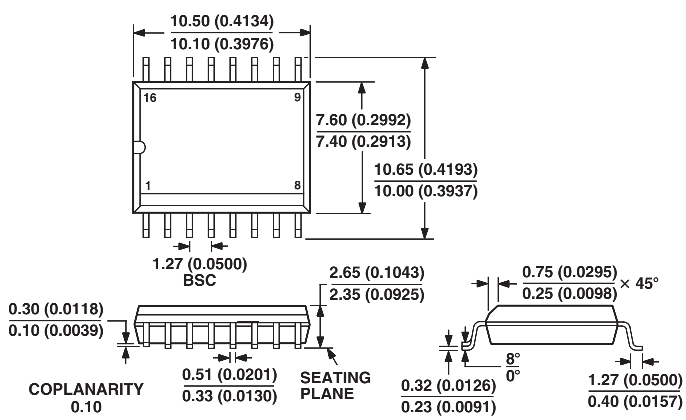


COMPLIANT TO JEDEC STANDARDS MO-095AA

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16-Lead Standard Small Outline Package [SOIC] Wide Body S-Suffix (RW-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AA

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Revision History

C00325–0–4/03(C)